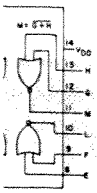
CP35

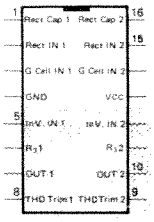
R Gate

Diagram

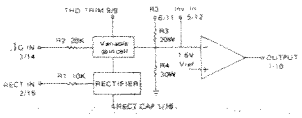


NE570
COMPANDER

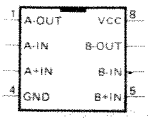
Block & Schematic Diagram



(TOP VIEW)

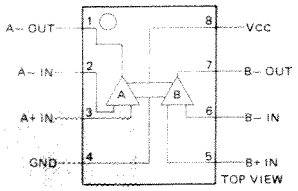


NJM4558DV
Dual Operational Amplifier

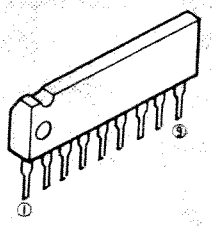


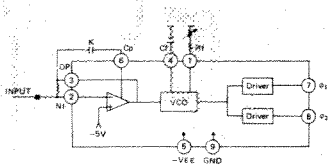
(TOP VIEW)

Logic Diagram



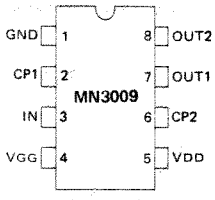
iG03290
BBD driver



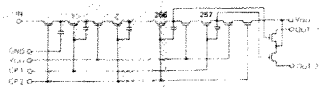


①	②	③	④	⑤	⑥	⑦	⑧	⑨
Rf	-IN	OP	Cf	V_{EE}	Cp	$\phi 1$	$\phi 2$	GND

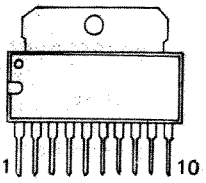
MN3009
256 stage BBD

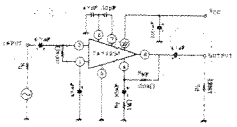


(Top View)



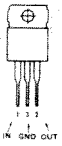
TA7220P
LOW POWER AMP.
P SIP 10 PIN (with Tab)

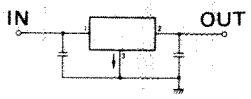




3pin: INPUT
8pin: OUTPUT

μPC14305H
μPC14315H
P 3 PIN





Pin No.	①	③	②
Pin Name	IN	GND	OUT
μPC14305H	10V		5V
μPC14315H	23V		15V

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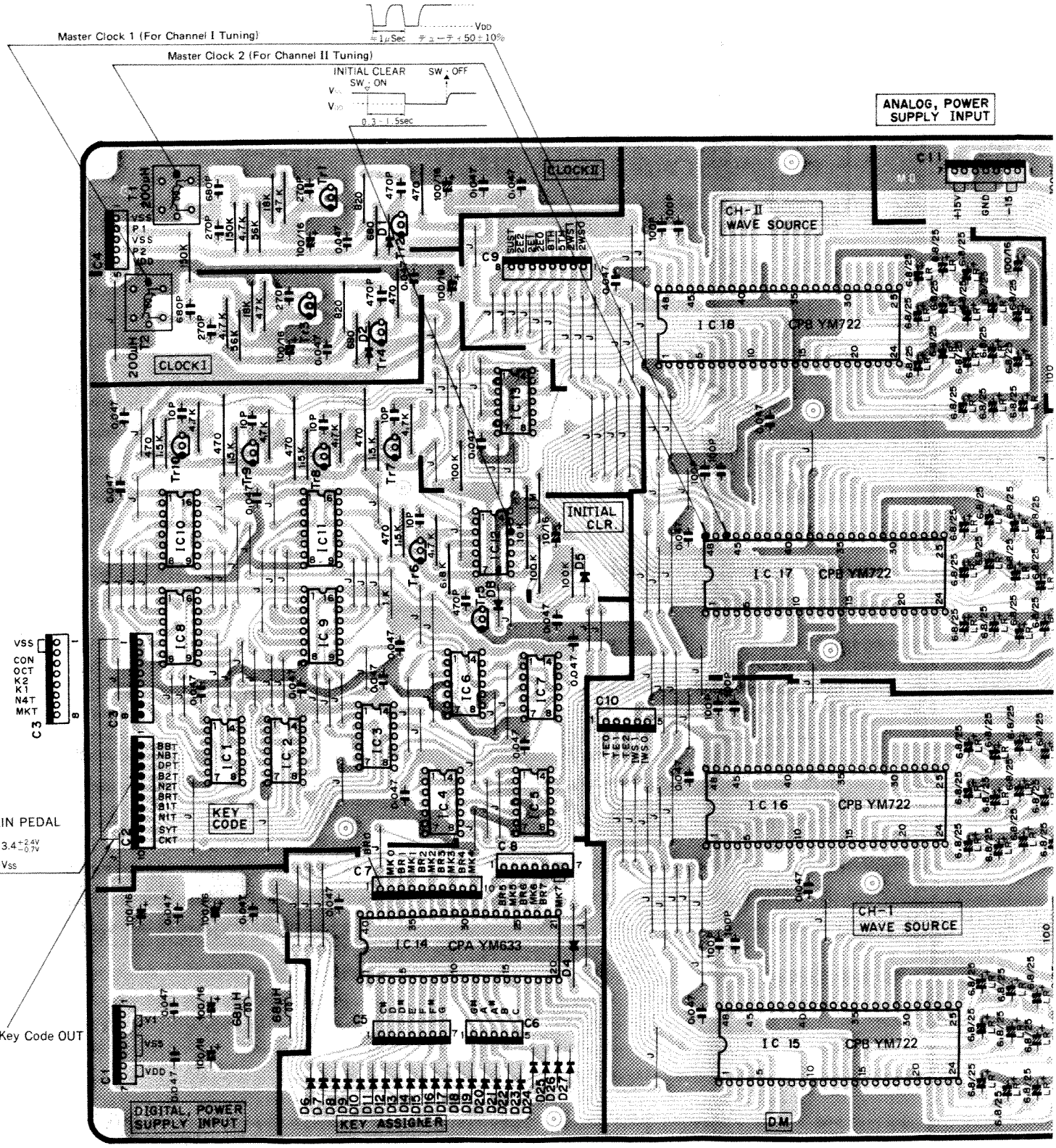
DM Circuit Board & Wining



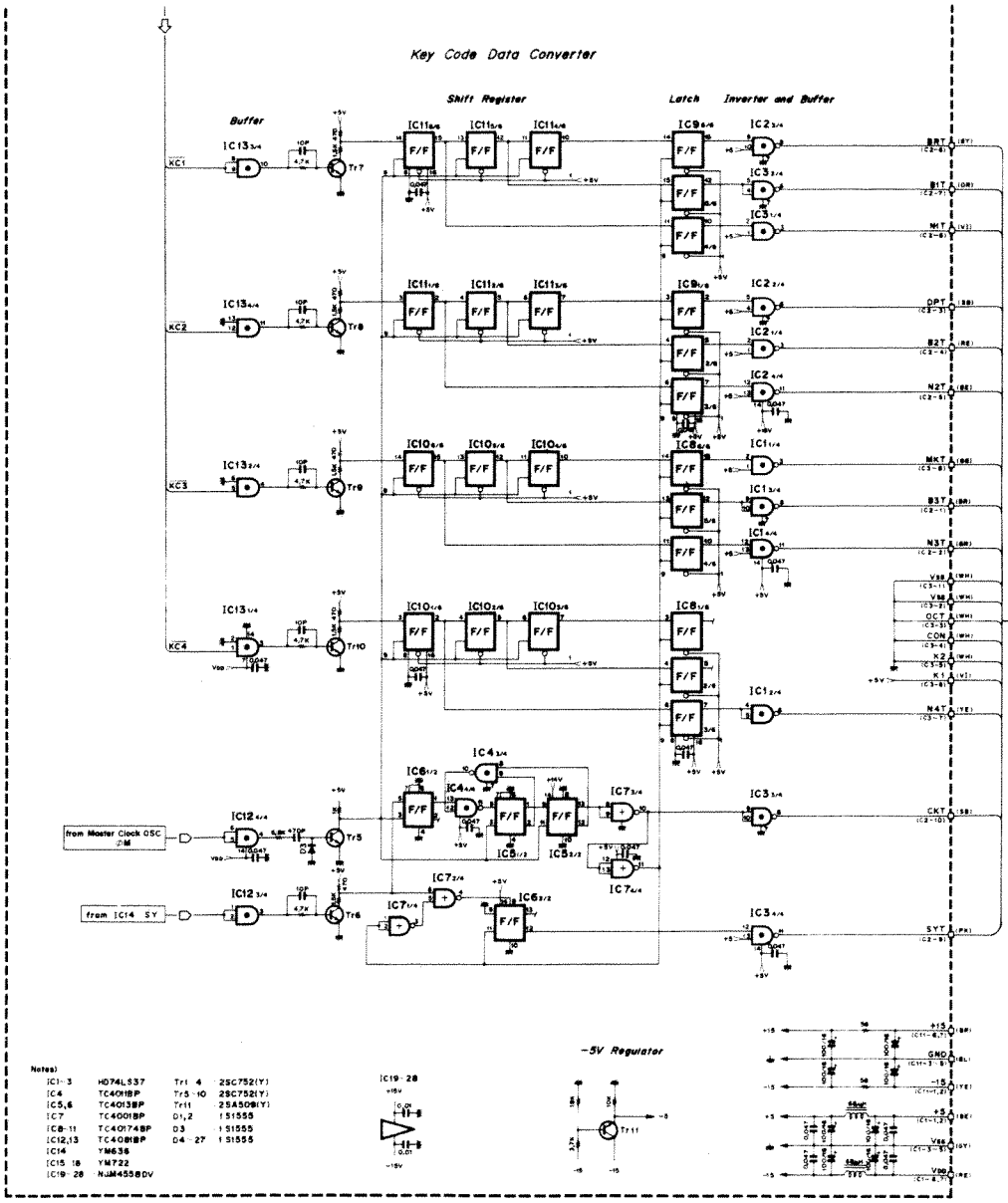
Component Side（部品側）

CP35

DM Circuit Diagram

(C3-2,4,6,8,10)
g/Filter II and Presets

(C5-2,4,6,8,10)
g/Filter II and Presets



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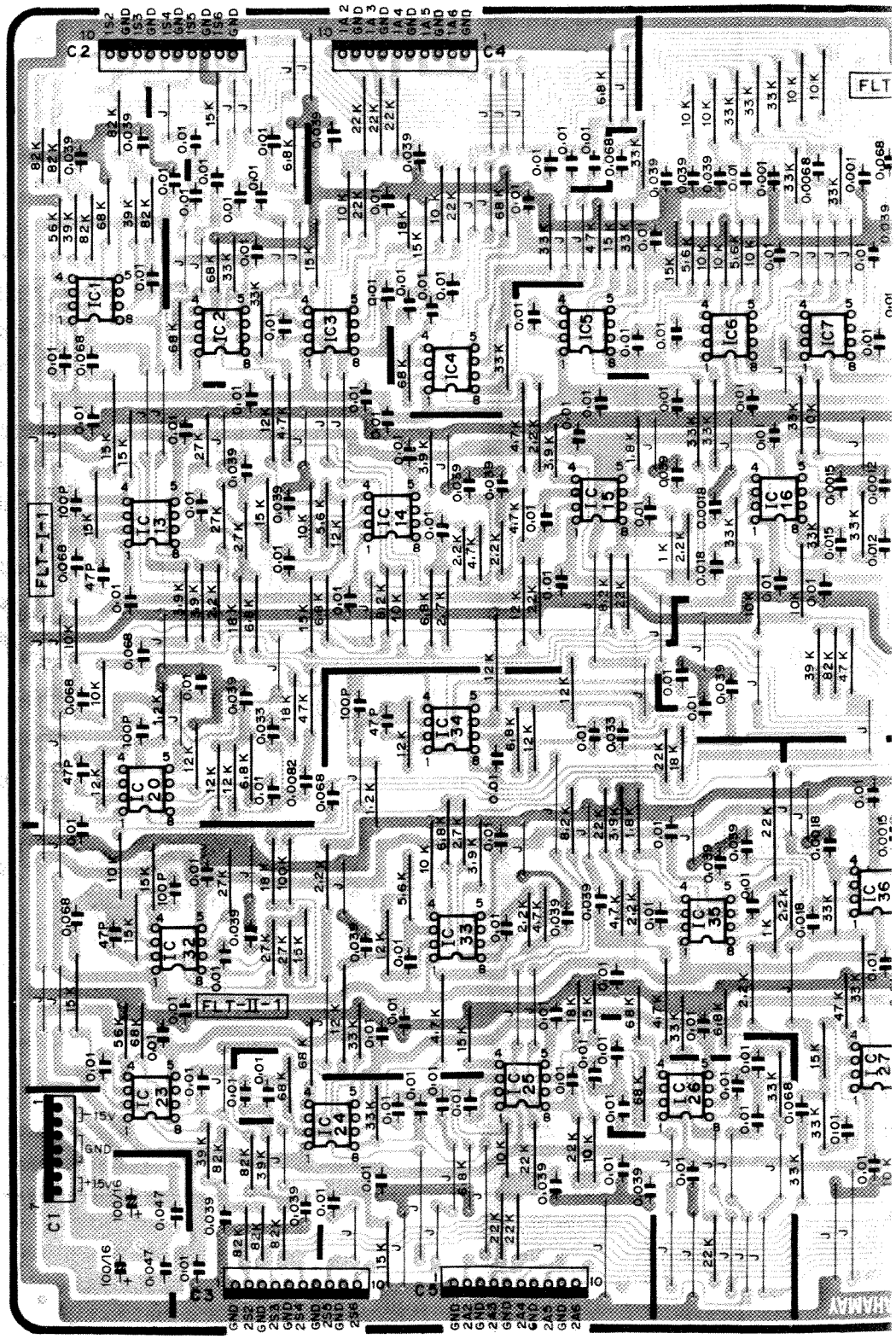
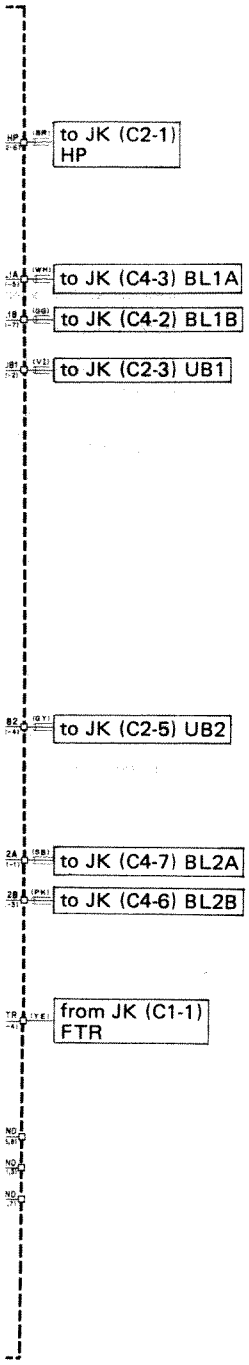
FL Circuit Board & Wining

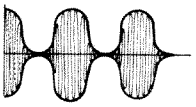
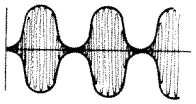
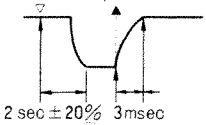


Component Side (部品側)

CP35

EFT Circuit Diagram



Item	Setting	Test Point	Adjustment	Adj. Point	Rem.
FLANGER OSC		IC5 pin 7	 f = 0.5 ± 0.3Hz		Check
		IC1 pin 7 pin 8	 f = 120kHz ~ 25kHz Make sure that FM mod. is applied in above freq. range.		Check
FLANGER WAVEFORM	FILTER I – 1 only on. Press C_5 key.	IC3 pin 10	 Adj. for perfect symmetry.	VR7	Adj.
TREMOLO OSC	TREMOLO SPEED –MAX	IC10 pin 7	 f = 15 ± 0.5Hz	VR1	Adj.
Speed	TREMOLO SPEED –MIN	IC10 pin 7	 f = 0.5 ± 0.4Hz		Check
Depth	TREMOLO DEPTH –MAX	IC11 pin 1			
	TREMOLO SW –ON	IC11 pin 1	Adjust for sine-wave.	VR2	Adj.
MODULATION BALANCE					
OUT 1		IC9 pin 1		VR3	Adj.
OUT 2		IC9 pin 7	 Adjust for 95% mod. Check that IC9 pin 1 is 180 degrees out of phase.	VR4	Adj.
UNBALANCED output circuit	FILTER I – 1 –ON	EQ (C3-6)	Adjust so 0.8 times the EQ terminal input signal appears at UB1, UB2.		
OUT 1	C_5 Key –ON	UB1 (C2-2)	power ON power OFF  2 sec ± 20% 3msec	VR5	Adj.
OUT 2		UB2 (C2-4)		VR6	Adj.
MUTING	Power	Tr6 Emitter			Check

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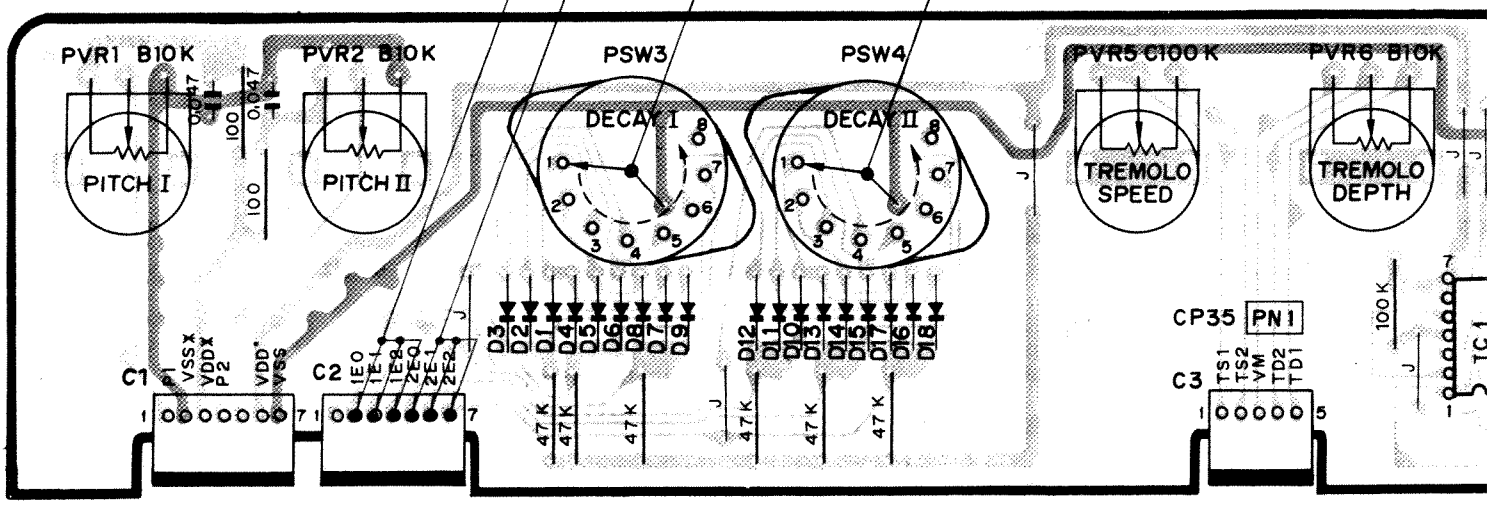
PN1, 4 Circuit Diagram

DECAY SW. Data

POSITION	1	2	3	4	5	6	7	8
$\overline{1E2}$ (C2–4) $\overline{2E2}$ (C2–7)	H	H	H	H	L	L	L	L
$\overline{1E1}$ (C2–3) $\overline{2E1}$ (C2–6)	H	H	L	L	H	H	L	L
$\overline{1E0}$ (C2–2) $\overline{2E0}$ (C2–5)	H	L	H	L	H	L	H	L

"H" =0V
"L" =−15V



- Connector

C1

Pin No.	Pin Name	Wire Color	Destination
1	P1	SB	DM-P1 (C4-2)
2	Vss*	WH	DM-Vss* (C4-3)
3	VDD*	OR	DM-VDD* (C4-5)
4	P2	PK	DM-P2 (C4-4)
5	–	–	
6	VDD°	PK	PN3-VDD° (C7-1)
7	Vss	GY	PN3-Vss (C7-3)

C2

Pin No.	Pin Name	Wire Color	Destination
1	*		–
2	$\overline{1E0}$	BR	DM-$\overline{1E0}$ (C10-2)
3	$\overline{1E1}$	RE	DM-$\overline{1E1}$ (C10-3)
4	$\overline{1E2}$	OR	DM-$\overline{1E2}$ (C10-4)
5	$\overline{2E0}$	YE	DM-$\overline{2E0}$ (C9-5)
6	$\overline{2E1}$	GR	DM-$\overline{2E1}$ (C9-6)
7	$\overline{2E2}$	BE	DM-$\overline{2E2}$ (C9-7)

C3

Pin No.	Pin Name	Wire Color	Destination
1	TS1	BE	EFT-TS1 (C5-3)
2	TS2	GR	EFT-TS2 (C5-2)
3	VM	WH	EFT-VM (C5-6)
4	TD2	GY	EFT-TD2 (C5-5)
5	TD1	VI	EFT-TD1 (C5-7)

C4

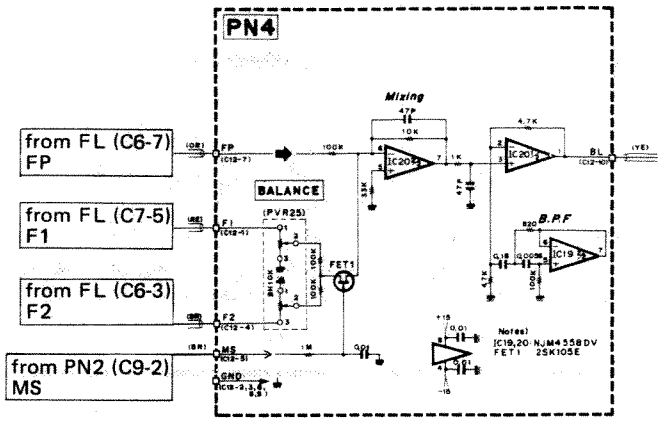
Pin No.	Pin Name	Wire Color	Destination
1	TR	OR	EFT-TR (C5-1)
2	FG	RE	EFT-FG (C3-3)
3	MS	BR	PN3-MS (C9-1)
4	PR4	PK	PN3-PR4 (C9-3)
5	PR3	SB	PN3-PR3 (C9-5)
6	PR2	GG	PN3-PR2 (C9-7)
7	PR1	WH	PN3-PR1 (C9-9)

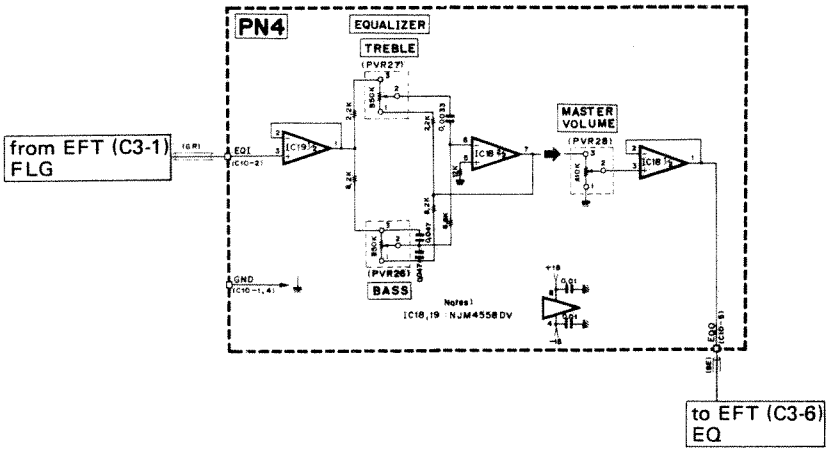
C5

Pin No.	Pin Name	Wire Color	Destination
1	–		–
2	$\overline{2WS0}$	WH	DM-$\overline{2WS0}$ (C9-1)
3	$\overline{1WS1}$	GY	DM-$\overline{1WS1}$ (C10-4)
4	$\overline{1WS0}$	VI	DM-$\overline{1WS0}$ (C10-5)
5	$\overline{2WS1}$	GG	DM-$\overline{2WS1}$ (C9-2)

CP35

PN4 Circuit Diagram





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MK1, 2, 3 Circuit Board & Wining, Circuit Diagram

C1

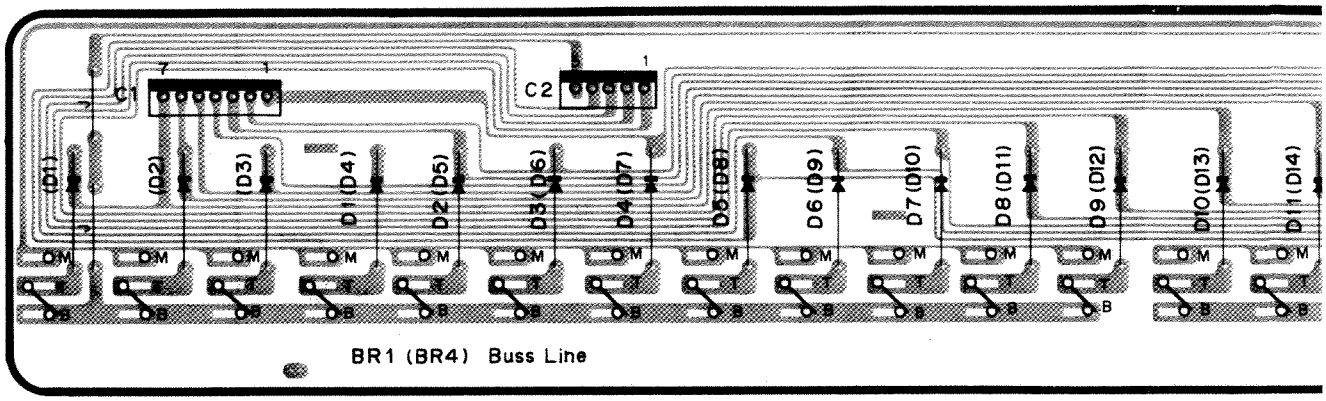
Pin	7	6	5	4	3	2	1
MK1	–	–	–	E	F	F#	G
(MK2)	C#	D	D#	E	F	F#	G

C2

Pin	5	4	3	2	1
MK1	G#	A	A#	B	C
(MK2)	G#	A	A#	B	C

C3

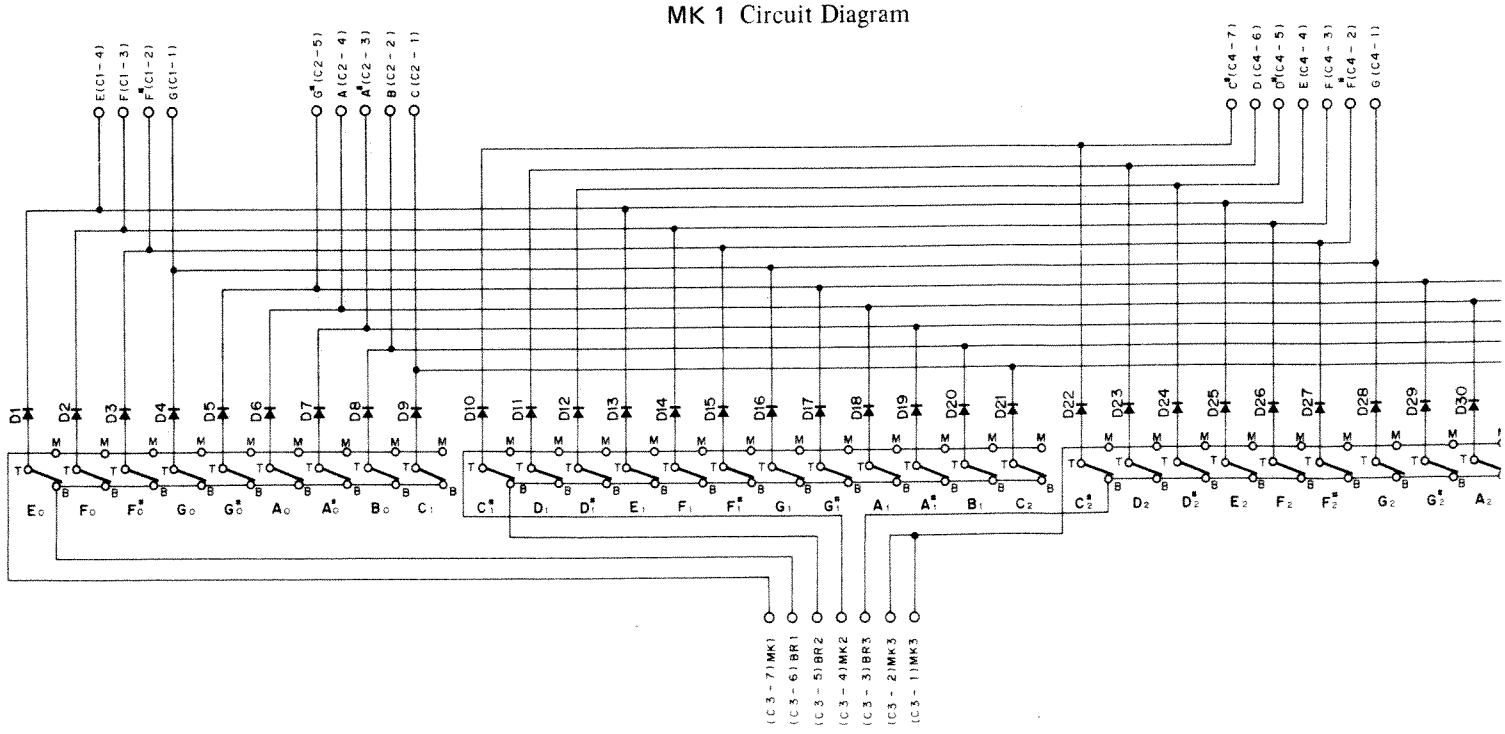
Pin	7	
MK1	MK1	B
(MK2)	MK4	B



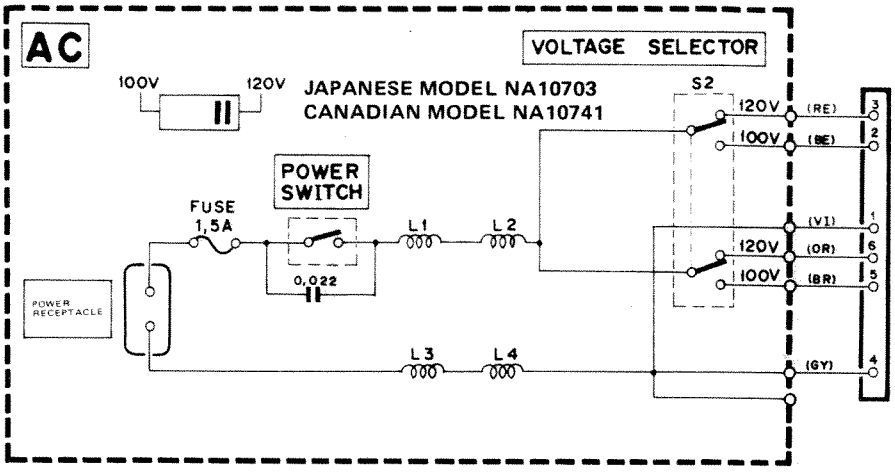
MK1 Board			E_0	F_0	$F^{\#}_0$	G_0	$G^{\#}_0$	A_0	$A^{\#}_0$	B_0	C_1	$C^{\#}_1$	D
(MK2 Board)	($C^{\#}_3$)	(D_3)	($D^{\#}_3$)	(E_3)	(F_3)	($F^{\#}_3$)	(G_3)	($G^{\#}_3$)	(A_3)	($A^{\#}_3$)	(B_3)	(C_4)	($C^{\#}_4$)	(D

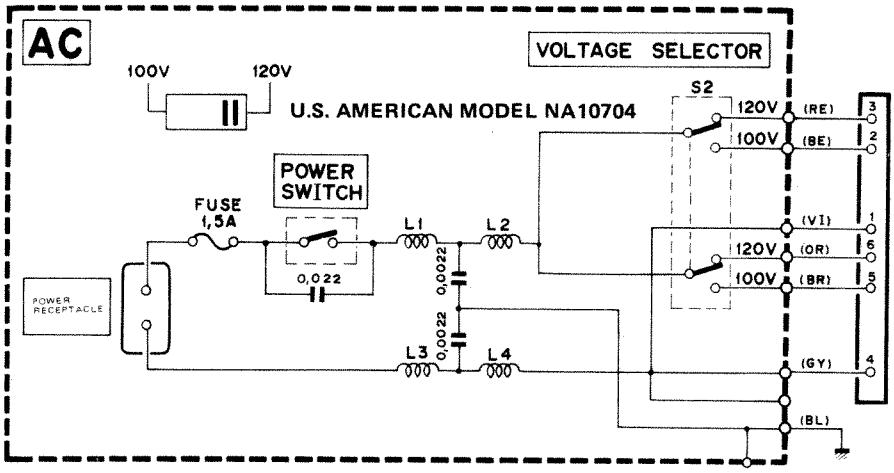
Component Side (部品側)

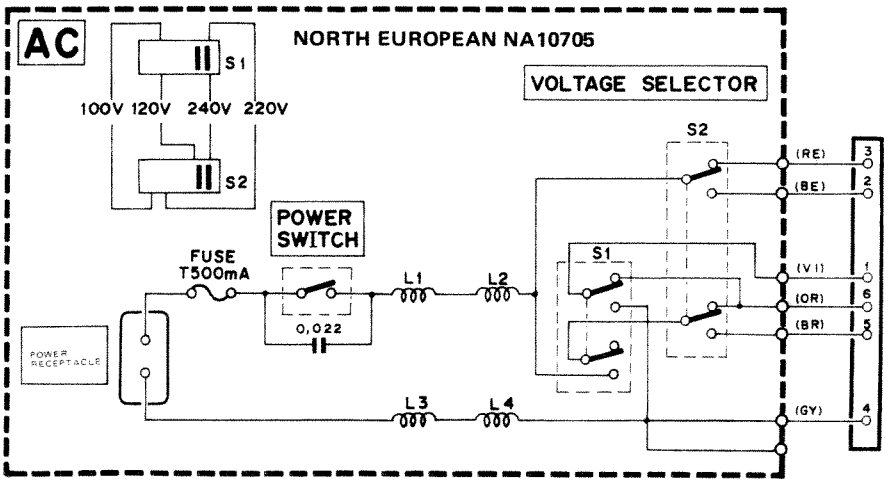
MK 1 Circuit Diagram



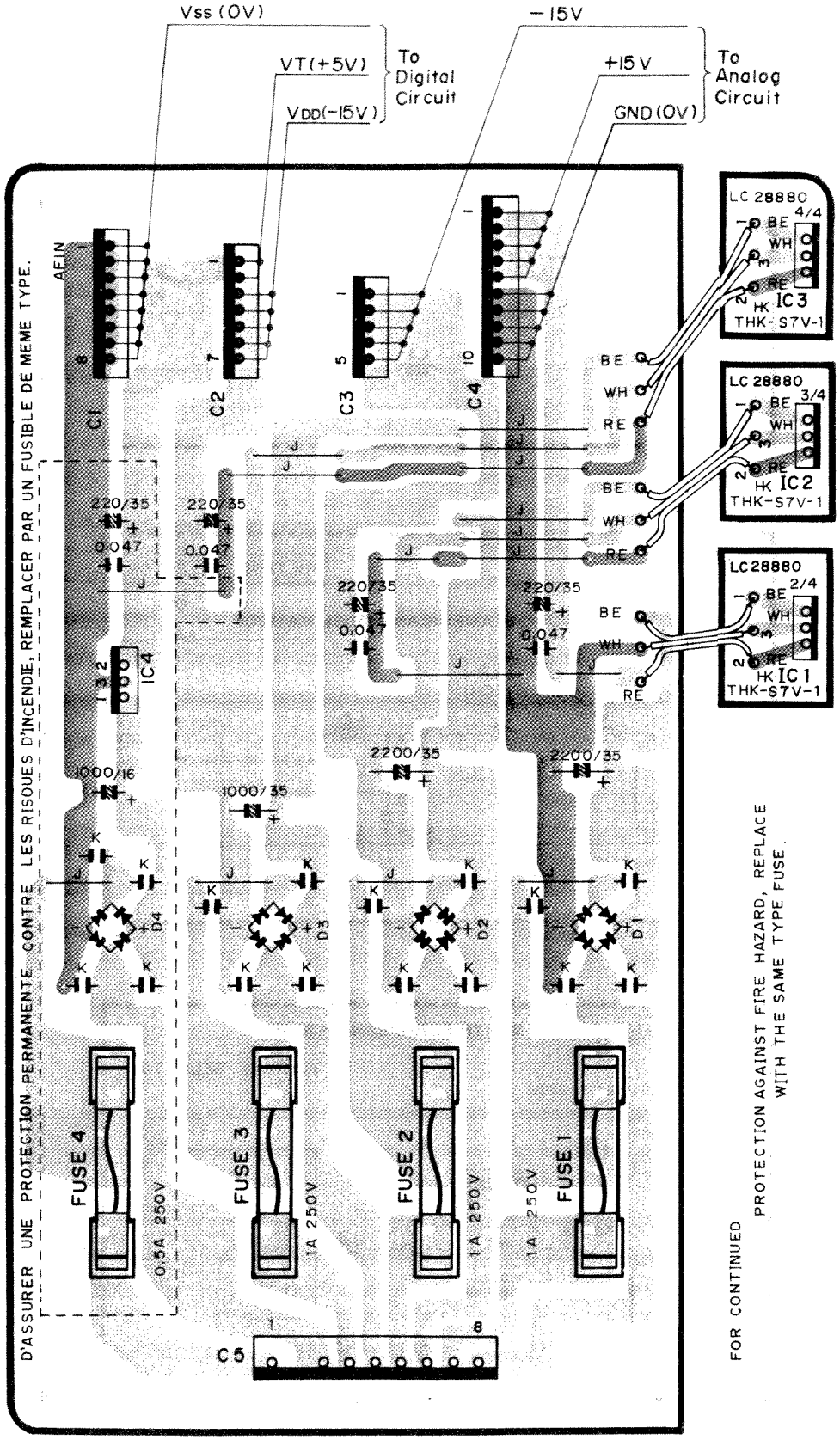
AC Circuit Board & Wining, Circuit Diagram







DC Circuit Board & Wining, Circuit Diagram



FOR CONTINUED

Component Side (部品側)

KEP-NA10697-14 ⚠0